CLAIMS

1. A method for fabricating a plurality of topologically different integrated circuits, said method comprising:

(a) fabricating a plurality of first integrated circuits, each first integrated circuit comprising N vertically stacked device layers L_1, L_2, ... L_N with a first set of photolithographic masks M_1, M_2 ... M_{MAX};

(b) fabricating a plurality of second integrated circuits, each second integrated circuit comprising M vertically stacked device layers L_1, L_2, ... L_M, where M<N, with a second set of photolithographic masks, wherein all of the photolithographic masks of the second set of masks used to form device layers L_1, L_2, ... L_{M-1} in (b) are included in the first set of masks used in (a).

2. The method of Claim 1 wherein the first and second integrated circuits comprise respective three-dimensional memory arrays, and wherein the devices of the first and second integrated circuits comprise memory cells.

3. The method of Claim 2 wherein each first integrated circuit has 2^j vertically stacked device layers, wherein each second integrated circuit has 2^k vertically stacked device layers, and wherein k<j.

4. The method of Claim 1 wherein the second set of masks includes only masks M_1, M_2 ... M_L, wherein L<MAX.

5. The method of Claim 1 wherein all of the photolithographic masks of the second set of masks used in (b) are included in the first set of masks used in (a).

6. A method for fabricating a plurality of topologically different integrated circuits, said method comprising:

(a) fabricating a plurality of first three-dimensional memory arrays, each first three-dimensional memory array having 2^j vertically stacked

memory cell layers L_1, L_2, ... L_2^j, with a first set of photolithographic masks M_1, M_2 ... M_{MAX};

(b) fabricating a plurality of second three-dimensional memory arrays, each second three-dimensional memory array having 2^k vertically stacked memory cell layers L_1, L_2, ... L_2^k, with a second set of photolithographic masks, wherein k<j, and wherein all of the photolithographic masks used to form memory cell layers L_1, L_2, ... L_2^{k-1} in (b) are included in the first set of masks used in (a).

7. The method of Claim 6 wherein j=3 and k=2.

8. The method of Claim 6 wherein all of the photolithographic masks used in (b) are included in the first set of masks used in (a).

9. A method for identifying a circuit, said method comprising:

(a) providing a plurality of integrated circuits, each integrated circuit comprising a plurality of vertically stacked device layers, a source, a sensing contact, and a conductive path extending across at least some of the stacked device layers, said integrated circuits comprising first ones of the integrated circuits, in which the conductive path interconnects the respective sensing contact and source, and second ones of the integrated circuits, in which the conductive path does not interconnect the respective sensing contact and source;

(b) supplying circuit identification signals selected from a first set with the first integrated circuits in response to sensed signals on the respective sensing contacts within a first range of values; and

(c) supplying circuit identification signals selected from a second set with the second integrated circuits in response to sensed signals on the respective sensing contacts within a second range of values.

10. The method of Claim 9 wherein the source is characterized by a source value, and wherein the source value is closer to the first range values than to the second layer of values.

11. The method of Claim 9 wherein the source and the sensing contact are disposed on different ones of the stacked device layers.

12. The method of Claim 9 wherein the source comprises a voltage source, wherein the sensed signal comprises a voltage signal, and wherein the first and second ranges of values are respective ranges of voltages.

13. A self-identifying circuit comprising:

an integrated circuit comprising a plurality of vertically stacked device layers, a source, a sensing contact, and a conductive path coupled with the sensing contact and extending across at least some of the stacked device layers, a parameter on the sensing contact indicative of whether the conductive path extends continuously between the sensing contact and the source;

a memory storing first and second sets of integrated circuit identification signals;

a switch responsive to the sensing contract, coupled with the memory, and operative (1) to select a circuit identification signal from the first set as an output when a sensed signal on the sensing contact is in a first range of values, and (2) to select a circuit identification signal from the second set as the output when the sensed signal on the sensing contact is in a second range of values.

14. The invention of Claim 13 wherein the source is characterized by a source value, and wherein the source value is closer to the first range of values than to the second range of values.

15. The invention of Claim 13 wherein the source and the sensing contact are disposed on different ones of the stacked device layers.

16. The invention of Claim 13 wherein the source comprises a voltage source, wherein the sensed signal comprises a voltage signal, and wherein the first and second ranges of values are respective ranges of voltages.

17. The invention of Claim 13 wherein the switch comprises a multiplexer.